CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a semiconductor layer;

a source region formed in the semiconductor layer;

a drain region formed in the semiconductor layer;

a channel region formed between the source region and the drain region in the semiconductor layer;

a gate insulating layer formed above the channel region; and

a gate electrode formed above the gate insulating layer,

wherein a boundary between the gate insulating layer and the channel region is a wave-like pattern of a gradual slope.

2. A semiconductor device comprising:

a semiconductor layer;

a source region formed in the semiconductor layer;

a drain region formed in the semiconductor layer;

a channel region formed between the source region and the drain region in the semiconductor layer;

a gate insulating layer formed above the channel region; and

a gate electrode formed above the gate insulating layer,

wherein a boundary between the gate insulating layer and the channel region is a wave-like pattern without any corners.

3. The semiconductor device according to Claim 1, wherein a pitch between a top of the wave-like pattern and an adjacent bottom of the wave-like pattern in the boundary is less than or equal to 50 nm.

4. The semiconductor device according to Claim 2, wherein a pitch between a top of the wave-like pattern and an adjacent bottom of the wave-like pattern in the boundary is less than or equal to 50 nm.

5. The semiconductor device according to Claim 1, wherein a part of an upper surface of the source region is flat.

6. The semiconductor device according to Claim 2, wherein a part of an upper surface of the source region is flat.

7. The semiconductor device according to Claim 5, wherein a part of an upper surface of the drain region is flat.

8. The semiconductor device according to Claim 6, wherein a part of an upper surface of the drain region is flat.

9. The semiconductor device according to Claim 1, wherein the semiconductor layer is formed above a support substrate with an insulating layer therebetween.

10. The semiconductor device according to Claim 2, wherein the semiconductor layer is formed above a support substrate with an insulating layer therebetween.

11. A method of manufacturing a semiconductor device comprising the steps of:

providing a substrate having a support substrate, an insulating layer, and a semiconductor layer in that order;

forming a mask layer having a plurality of openings at predetermined intervals above the semiconductor layer;

selectively thermal oxidizing the substrate in an oxidizing ambient so as to form a waveform oxide layer with a pattern of a gradual slope above the semiconductor layer;

removing the mask layer;

removing the oxide layer;

forming a gate insulating layer above the semiconductor layer;

forming a gate electrode above the gate insulating layer; and

forming a source region and a drain region by doping an impurity into the semiconductor layer using at least the gate electrode as a mask.

12. A semiconductor device comprising:

a semiconductor layer;

a source region formed in the semiconductor layer;

a drain region formed in the semiconductor layer;

a channel region formed between the source region and the drain region in the semiconductor layer;

a gate insulating layer formed above the channel region; and

a gate electrode formed above the gate insulating layer,

wherein a boundary between the gate insulating layer and the channel region undulates.

13. The semiconductor device according to Claim 12 wherein said boundary undulates in a sinusoidal pattern.

14. The semiconductor device according to Claim 12 wherein said boundary undulates in a curving pattern.